REMARKS / DISCUSSION OF ISSUES

Claims 1-8 are pending. Claims 1 and 7 are independent.

Applicants have again considered the request for subject headings and again respectfully decline the inclusion thereof.

Claim 5 has been amended to address the objection thereto, rendering this objection moot.

Objection to the Specification

The Office Action alleges that the title "DATA PROCESSING SYSTEM WITH CLUSTERED ILP PROCESSOR" is non-descriptive and thus not indicative of the claimed subject matter. At the outset, there is no basis in law provided, or any standard thereof provided in support of this objection. Accordingly, and if for no other reason, Applicants respectfully submit that this objection is without merit and must be withdrawn.

The above notwithstanding, Applicants note, for example, that claim 1 is drawn to a data processing system and features:

"...a clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;"

Applicants thus submit that the title is ethereal or non-descript, but rather highly descriptive of the claimed subject matter of at least claim 1.

For at least the reasons set forth above, Applicants respectfully submit that the objection to the title/specification is improper and should be withdrawn.

Rejections under 35 U.S.C. § 112, ¶ 2

Claims 1-8 are rejection under section 112 of the Code for alleged indefiniteness. Applicants respectfully disagree, and not that the application as filed clear discloses this question relationship.

The Examiner asserts:

b. In claim 1, lines 9-10 and claim 5, lines 9-10, the applicant's amended claims disclose "said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters." It is indefinite as to how a pipeline register may solely provide a connection between any two of said clusters, as opposed to the connection between the instruction unit and the clusters, which is connected by both a pipeline register and respective control connections. Furthermore, it is indefinite as to if the same pipeline registers are being used as part of both the control connections and the data connections, or whether a subset of the pipeline registers are being used for one type of connection, and the remaining pipeline registers for the other type of connection.

A connection of cluster according to an embodiment described in the filed application is described:

"In Fig. 1 a clustered VLIW architecture with a full point-to-point connectivity topology according to a first embodiment is shown. The architecture includes four clusters, namely clusters **A, B, C and D, which are fully connected to each other and an instruction fetch/dispatch unit IFD being connected to each cluster A-D via control connections paths CA-CD.** Accordingly, **there is always a dedicated direct data signal connection present between any two clusters with pipeline registers P arranged between each two clusters.** The latency of an inter-cluster transfer of data is always the same for every inter-cluster connection independent of the actual distance between the clusters on the chip. The actual distance on the chip between the clusters A and C, and clusters B and D is considered to be longer than the distance between the clusters A and D, A and B, B and C, as well as C and D. Therefore, a pipeline register P is arranged in the control connection paths CC and CD,

in order to pipeline the control signals to remote clusters C, D."

(Emphasis Provided).

From the description in the filed application in which the signal connection featured in claim 1 is provided in *ipsis verbis* to the claim language, one can garner how the dedicated signal connection is realized.

Accordingly, and for at least the reasons set forth in above, Applicants respectfully submit that the dedicated direct signal connection between any two clusters is well within the requirements of 35 U.S.C. § 112, ¶ 2. Therefore, Applicants respectfully traverse this rejection as being improper.

Rejections under 35 U.S.C. § 103(a)

Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being obvious in view of *Batten, et al.* (U.S. Patent 6,269,437) and *Nickolls, et al.* (U.S. Patent 5,598,408). Applicants have reviewed this rejection and respectfully submit that the rejection is improper for at least the following reasons:

Claims 1 and 5, as amended, include pipeline registers, *the pipeline registers are adapted to provide a dedicated direct signal data signal connection between any two of the clusters*.

In Fig. 1 of the filed application, a clustered VLIW architecture with a full point-to-point connectivity topology according to a first embodiment is shown. The architecture includes four clusters, namely clusters A, B, C and D, which are fully connected to each other and an instruction fetch/dispatch unit IFD being connected to each cluster A-D via control connections paths CA-CD. Accordingly, there is always a dedicated direct data signal connection present between any two clusters with pipeline registers P arranged between each two clusters.

The Office Action directs Applicants to column 10, lines 25-26 and lines 31-35 in asserting that the noted feature of claim 1 is taught by *Batten, et al.* Applicants respectfully disagree.

The reference to *Batten, et al.* discloses in the Abstract that:

[T]he processor includes multiple clusters of execution units, with each of the clusters having a portion of a register file and a portion of a predicate file associated therewith, such that a given cluster is permitted to write to and read from its associated portions of the register and predicate files. A duplicator interconnection technique in accordance with the invention reduces port pressure by providing one or more global move units in the processor. A given global move unit uses an inter-cluster move instruction to copy a value from a portion of the register or predicate file associated with a source cluster to another portion of the register or predicate file associated with a destination cluster.

A review, for example of Fig.12 of the filed application reveals no dedicated connection between clusters. Moreover, the cited portion of column 10 fails to disclose the dedicated connection between clusters. Finally, the portion of the Office Action reproduced presently does not present evidence of such as connection. To wit, the Office Action states:

and said pipeline registers being adapted to provide a dedicated direct signal connection between any two of said clusters (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity, requiring additional move instructions; col. 3, line 23-43 go into detail about the arrangement).

At the outset, organizations O1 and O2 include branch units, memory units and a prescribed number of ALUs. The Office Action fails to articulate clearly the disclosure in the reference of connections between clusters are dedicated as claimed. Finally, a review of column 3, lines 23-43 fail to elucidate the alleged dedicated connection either. Rather the need to specify the degree of access and method of communication between clusters is disclosed; without disclosure of a dedicated connection.

Accordingly, because the applied art fails to disclose at least one feature of independent claim 1 and independent claim 5, a *prima facie* case of obviousness cannot be made based thereon. Thus, claims 1 and 5 are patentable over the applied art. Moreover, claims 2-4 and 6-8, which depend from claims 1 and 5, respectively, are patentable at least for the same reasons as claims 1 and 5. Allowance is earnestly solicited.

Finally, the Office Action offers reasons for combining references in the rejection under 35 U.S.C. § 103(a). Applicants silence on the propriety of these combinations is by no means indicative of their acquiescence thereto. Applicants reserve their right to address any issues regarding the propriety of these combinations in further correspondence as needed.

Conclusion

In view the foregoing, applicant(s) respectfully request(s) that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees, including, but not limited to, the fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

If any points remain in issue that may best be resolved through a telephonic interview, the Examiner is respectfully requested to contact Eric M. Bram, Esq. at (914) 945-6000.

Respectfully submitted on behalf of:

Phillips Electronics North America Corp.

by: William S. Francos (Reg. No. 38,456)

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Volentine Francos & Whitt, PLLC
Two Meridian Blvd.
Wyomissing, PA 19610
(610) 375-3513 (v)
(610) 375-3277 (f)